## REMARKS

Claims 1-27 are pending in the application. By this Amendment, claims 1, 10, 15 and 16 are amended. Applicant has not received an indication whether the amendments filed February 6, 2005 have been entered. Therefore, the above amendments amends claims 1, 10 and 16 in a similar manner as in the February 6 response. Additionally, each of independent claims 1, 1- and 16 are also amended to recite features such as "relating to the resetting of the processors."

Applicant gratefully acknowledges the courtesies extended by Examiner Delgado during the telephonic interview on February 28. As specifically discussed during the interview, the above amendments generally reciting "relating to the resetting of the processors" overcomes the outstanding rejection. Further, as discussed during the interview, the outstanding rejection based at least on U.S. Patent 5,655,079 to Hirasawa should be withdrawn and a new search should be conducted if necessary.

Applicant respectfully submits that the finality of the October 5 rejection is improper and should be withdrawn. More specifically, the Office Action (on page 3, for example) relies on features relating to determining whether accessed information has an error and an IPC format. However, these features were previously recited within the claims. Therefore, applicant's amendment filed on July 6, 2005 did not necessitate the new search and/or new grounds of rejection based on U.S. Patent 5,655,079 to Hirasawa. Since applicant's amendment did not necessitate the new search and/or the new grounds of rejection, the finality of the Office Action should be withdrawn.

Entry of this Amendment is proper under 37 C.F.R. §1.116 because the amendments: a) place the application in condition for allowance for the reasons set forth below; b) do not raise any new reasons that require further search and/or consideration; and c) place the application in better form for an appeal should an appeal be necessary. More specifically, the amendment to claim 1 is to correct a typographical error, and the amendment to claim 15 is merely for clarity. Claims 1, 10 and 16 are also amended in a manner as discussed during the telephonic interview. No new issues are raised. Thus, entry of this Amendment is proper under 37 C.F.R. §1.116.

Applicant gratefully acknowledges the Office Action's indication that claims 6-9, 12-14 and 21-24 contain allowable subject matter. However, for at least the reasons set forth below, all claims are believed to contain allowable subject matter.

The Office Action rejects claims 1-5, 10-11, 15-20 and 25-27 under 35 U.S.C. §103(a) over U.S. Patent 6,401,200 to Nishiike et al. (hereafter Nishiike) in view of U.S. Patent 5,655,079 to Hirasawa et al. (hereafter Hirasawa). The rejection is respectfully traversed.

Independent claim 1 recites requesting an information down-load from the lower processors to the upper processor and transferring the IPC format information from the upper processor to the lower processors by using the group representative address, the transferred IPC format information including the accessed information relating to the resetting of the processors and the group representative address.

The Office Action (on page 3) appears to state that Nishiike does not teach or suggest various features of the claims such as at least the claimed determining and the claimed

transferring. The Office Action appears to rely on Hirasawa as teaching the claimed determining and transferring.

As expressly discussed during the interview, Hirasawa clearly does not suggest the transferred IPC format information including the accessed information relating to the resetting of the processors and the group representative address. The rejection should be withdrawn at least for this reason (as was discussed during the interview).

Applicant respectfully submits that Nishiike and Hirasawa may not be combined as alleged in the Office Action. That is, there is no suggestion and/or motivation for combining Nishiike and Hirasawa as alleged. Applicant also respectfully submits that Nishiike and Hirasawa, even if combined, still do not teach or suggest all the features of independent claim 1 (as well as the other independent claims).

Nishiike relates to a controller 200 that supplies write enable signals to instruction memories 131, 132 and 133 and supplies an address generator 220 with an instruction for generating the address. The address generator 220 may generate addresses that are supplied to selectors 141, 142 and 143 and are supplied to the master ROM 230. Then, data stored in the master ROM 230 specified by the address may be read therefrom and written to the instruction memories 131, 132 and 133. After writing the necessary download information to the instruction memories, the controller 200 generates boot permission signals to the DSPs 111, 112 and 113. The DSPs 111, 112 and 113 read the download information stored in the instruction memories 131, 132 and 133 and store the read download information therein.

In contrast, Hirasawa relates to a data transmission method for a multi-computer system that has a plurality of computers connected via a transmission line. See, for example, Hirasawa's Abstract and Figure 9. Hirasawa is different than Nishiike's system relating to a plurality of DSPs to which instruction memories are provided. That is, Hirasawa relates to different computers transferring messages between one another across a transmission line. Hirasawa's col. 7, lines 37-47 states that each computer may transmit a message and may decide whether to receive data or not according to a group address and a content code. However, there is no suggestion of how Hirasawa's group address and content code that are provided for a plurality of computers interconnected by a transmission line may be incorporated into Nishiike's disclosure relating to a plurality of DSPs.

Nishiike's plurality of DSPs 111, 112, 113 are not coupled by a common transmission line. Rather, specific addresses may be addressed for each of the DSPs based on signals applied to the selectors 141, 142 and 143. The data may be provided to each of the DSPs 111, 112, 113 from the master ROM 203. There is no suggestion of how this may be modified so as to incorporate Hirasawa's group address signal and/or content code. In other words, Nishiike describes a specific technique for supplying data to a plurality of DSPs. The alleged modification would clearly destroy the express purpose of Nishiike's system. MPEP § 2143.01 clear states that if a proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. See *In re Gordon*, 221 USPQ 1125 (Fed. Cir. 1984). The modification

alleged in the Office Action would clearly destroy the operations of Nishiike. Thus, the alleged combination is improper.

Also, Nishiike discloses that data from master ROM 230 is written to the instruction memories. However, independent claim 1 recites that the transferred IPC format information includes the accessed information and the group representative address. Even if the references are combined as alleged, there would be no suggestion to transfer a group representative address from the master ROM 230 to the instruction memories and ultimately to the DSPs. Nishiike clearly describes the transfer of data and has no suggestion for the transfer of a group representative address.

For at least the reasons set forth above, the combination, even if made, does not teach or suggest transferring the IPC format information from the upper processor to the lower processors by using the group representative address, the transferred IPC format information including the accessed information relating to the resetting of the processors and the group representative address.

Still further, the Office Action appears to assert that Nishiike's controller corresponds to the claimed upper processor and Nishiike's DSPs correspond to the claimed lower processors. The Office Action (on page 2) also asserts that Nishiike discloses requesting information download from the lower processors to the upper processor. The Office Action cites Nishiike's col. 1, lines 5-15 as well as states that Nishiike's boot process is initiated by DSPS. However, applicant respectfully disagrees. Nishiike's boot process is described at col. 5, lines 1-25. As is clearly set forth in this section, various operations (such as downloading information into

instruction memories) are performed and then the controller 200 issues boot permission signals to the DSPs 111, 112 and 113. After the DSPs receive the download information, then the DSPs send the boot complete signals to the controller 200. This clearly does not suggest the claimed requesting an information down-load from the lower processors to the upper processor. Additionally, col. 1, lines 5-15 clearly does not state that the DSPs initiate a boot process as alleged in the Office Action. Thus, the combination does not teach or suggest all the claimed features.

For at least the reasons set forth above, Nishiike and Hirasawa do not teach or suggest all the features of independent claim 1. Accordingly, independent claim 1 defines patentable subject matter.

Independent claim 10 recites transmitting a request for an information down-load from the plurality of second processors to the first processor and transferring the assembled requested information from the first processor to at least two second processors using a group representative address, the transferred assembled requested information including the accessed information relating to the resetting of the processors and the group representative address. For at least similar reasons as set forth above, Nishiike and Hirasawa may not be combined as alleged. Further, even if combined, the combination of Nishiike and Hirasawa does not teach or suggest all these features of independent claim 10. Nishiike also does not suggest the claimed transmitting a request for an information down-load from the plurality of second processors to the first processor. That is, Nishiike's DSPs do not transmit a request for an information down-load to the controller 200. Thus, independent claim 10 defines patentable subject matter.

Still further, independent claim 16 recites transferring the requested information in the IPC format from the first processor to the plurality of second processors based on the representative address of the plurality of second processors, the transferred information in the IPC format including the requested information relating to the resetting of the processors and the representative address of the plurality of second processors. For at least similar reasons as set forth above, Nishiike and Hirasawa do not teach or suggest all these features. Additionally, for at least similar reasons as set forth above, Nishiike does not suggest the claimed requesting information from a first processor. Thus, independent claim 16 defines patentable subject matter.

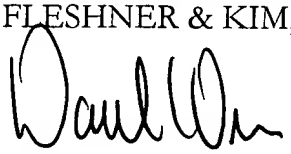
As stated above, each of independent claims 1, 10 and 16 defines patentable subject matter. Each of the dependent claims depends from one of the independent claims and therefore defines patentable subject matter at least for this reason. In addition, the dependent claims recite features that further and independently distinguish over the applied references.

## CONCLUSION

In view of the foregoing, it is respectfully submitted that the application is in condition for allowance. Favorable consideration and prompt allowance of claims 1-27 are earnestly solicited. If the Examiner believes that any additional changes would place the application in better condition for allowance, the Examiner is invited to contact the undersigned attorney at the telephone number listed below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this, concurrent and future replies, including extension of time fees, to Deposit Account 16-0607 and please credit any excess fees to such deposit account.

Respectfully submitted,
FLESHNER & KIM, LLP



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